Notice of Allowability	Application No.	Applicant(s)	
	10/656,982	SAKHUJA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt (Jun 2, 2005) and Interviews (Jun 15 & 17, 2005)*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☒ The drawings filed on *Sep 5, 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *06172005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicants' representative E. Eric Hoffman (Reg. No. 38,186) on Jun 17, 2005.

The application has been amended as follows:

Claim 22, line 13: changed "a" to --the--;

line 18: changed "transistor" to --transistor, effectively comparing the test voltage to the reference voltage as represented by the charge provided on the floating gate--;

Claim 25, line 21: changed "transistor" to --transistor, wherein the second transistor functions as the storage transistor which effectively stores the programmed reference voltage"; and

Claim 27, line 27: changed "transistor" to --transistor, effectively comparing the test voltage to the reference voltage as represented by the charge provided on the floating gate--.

Line 13 of claim 22 was changed to relate the "second transistor" back to the "second transistor" already recited on lines 7 and 9 of the same claim. The other changes (i.e. to claims 22 (line 18), 25, and 27) were made to provide more structural, and/or functional, relationships between some of the recited limitations. For example, although the preamble of claim 22 cites

"comparing a test voltage to a reference voltage", and the body of the claim recites "the reference voltage" and "the test voltage", the comparing step recited on the unamended claim's lines 16-17 only compare the source voltages of the first and second transistors. Therefore, the relationships between the two comparisons was not clear, and the claim was amended to relate the compared source voltages to the compared test and reference voltages. For example, using the applicants' own Fig. 1 as a reference, the source voltages of transistors 110 and 130 are compared by comparator 180, wherein voltage V_IN is understood to correspond to the test voltage, and the voltage stored on transistor 110 (e.g. stored during programming). Therefore, the compared source voltages effectively correspond to the compared test voltage and reference (e.g. stored) voltage. Claims 25 and 27 were amended for the same type of reasoning described above with respect to claim 22.

RESPONSE TO THE AMENDMENT

The amendment submitted on Jun 2, 2005 was reviewed and considered with the following results:

The amended paragraphs overcame the various objections to the disclosure that were described on page 2 of the previous Office Action. Therefore, those objections have all been withdrawn.

Amended claims 19 and 20 overcame the objections of claims 20-21, which have also been withdrawn.

Amended claims 1, 5-7, 10, 14-15, 17, 19-20, 25, 27, and 30 overcame all the rejections of claims 1-21, and 25-30 described in the previous Office Action. Those rejections have now been withdrawn. [Note: Although claim 22 was amended, its change removed "floating" from

"floating gate" with respect to the second transistor. That particular change was not made to address/correct any formal objection or rejection identified by the examiner in the previous Office Action.]

Amended claim 1 overcame the rejections of claims 1-2, and 4-5 under 35 U.S.C. 103(a) with respect to Pathak et al./Madurawe et al. Those rejections have all been withdrawn because neither reference clearly shows or discloses the input terminal being coupled to the drains of the first and third transistors, as well as to the second gate of the third transistor, as now recited within independent claim 1.

When all the active claims were carefully reviewed and considered, it was noted that several claims did not clearly relate their method steps to their preamble (e.g. "comparing a test voltage to a reference voltage" in the preamble of both claims 22 and 27; and claim 25's "programming a reference voltage into a storage transistor"). Since this could cause potential problems (i.e. confusion), the changes described in the Examiner's Amendment above were made to help clarify/relate the claimed method steps with wording already cited within the claim's preamble.

Previous non-elected claims 31-34 (with respect to a restriction requirement) have now been cancelled.

There is no known objection or rejection remaining within the present application.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses: A) the integrated circuit, or voltage reference circuit, as recited within independent apparatus claims 1

or 15; or B) the methods for creating a reference voltage circuit, comparing a test voltage to a reference voltage, or programming a reference voltage into a storage transistor, as recited within independent method claims 10, 22, 25, or 27. More specifically, none of the references clearly shows or discloses: 1) the input terminal being coupled to the drains of the first and third transistors, as well as to the second gate of the third transistor, as recited within claim 1 (upon which claims 2-9 depend); 2) electrically connecting the drains of the first and third transistors, and the second gate, wherein the second gate (located over the first gate) is also electrically connected to the first gate, as recited within claim 10 (upon which claims 11-14 depend); 3) the first/second transistors are connected between the input terminal and the respective first/second inputs of a comparator as recited within claim 15 (upon which claims 16-21 depend), wherein the second gate is located over, and electrically connected to, the first gate; 4) the test voltage is supplied to the drains of the first and second transistors, and to the gate of the second transistor, wherein the comparison of the source voltages of the first and second transistors effectively compares the test voltage and reference voltage, as recited within claim 22 (upon which claims 23-24 depend); 5) the reference voltage is supplied to the drains of the first and second transistors, and to the first gate of the third transistor, wherein a programming potential across the first transistor is removed when the second transistor's output becomes equal to the third transistor's output as recited within claim 26 (upon which claim 26 depends); and 6) the test voltage is supplied to the test voltage input terminal, coupled to the first terminal of both the first and second transistors, wherein the comparison of the outputs of the first and second transistors effectively compares the test voltage and reference voltage, as recited within claim 27 (upon which claims 28-30 depend) are compared. Since there is no strong motivation to modify or

combine any prior art reference(s) to ensure all of the claimed limitations, especially those described above, are met within any of the independent claims, the claims are deemed patentably distinct over the prior art of record.

Therefore, claims 1-30 are allowed, and previously withdrawn claims 31-34 have been cancelled.

Any comments considered necessary by the applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Terry L. Englund
17 June 2005